IOSR Journal of Electrical and Electronics Engineering (IOSR-JEEE)
e-ISSN: 2278-1676,p-ISSN: 2320-3331, Volume 12, Issue 4 Ver. III (Jul. – Aug. 2017), PP 44-59
www.iosrjournals.org

Design of a Controllable Adder-Subtractor circuit using Quantum Dot Cellular Automata

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Abstract: *Quantum Dot Cellular Automata (QCA) is a new paradigm in Nanotechnology that has grown much interest in the past few years. As the digital circuit's dimension have been reducing at a fast pace, basic components of a CMOS based transistor less circuit size has to be decreased accordingly. But it leads to certain unavoidable problems. Here comes the benefit of QCA, as it can be used efficiently in far smaller chips. This paper proposed a new concept of Controllable Layered Adder and Subtractor circuit which is the basic building block of any arithmetic and logic design using QCA. The design specifies that without making any changes the same circuit provides two different outputs by the application of different clock pulses to a particular cell. Proposed design idea is suitable for Adder and Subtractor designs where combine output is required in nano scale level. The design approach is applied in a two bit multiplier based ALU circuit as an application. Estimation of Kink Energy, effective area, Operation cost, Area Utilization Factor and latency has been done to the circuits.*

Keywords: *Area utilization factor, Controllable Adder Subtractor, Kink energy, latency, Operation cost.*

Date of Submission: 25-07-2017 Date of acceptance: 14-08-2017

I. Introduction

CMOS technology has played the pivotal role in the world of the digital electronics circuit designing. Area and complexity are two main issues in CMOS based VLSI design. In CMOS based design if gate length is below 10nm performance of the devices decreases due to quantum mechanical effect and its gate leakage current increases. Further size reduction will not be able to yield reliable output. The energy-inefficient structure of complex designs in Nano-scale increases difficulty in lithography [1, 2]. Again, in case where the circuit need to work faster and consume less power, which usually doesn't happen in case of CMOS circuits because it tends to use more power in high speed structures [3,4]. Hence, designers are in search of an alternative to the conventional CMOS technology to achieve compact and integrated design with low power dissipation. Among the possible substitutes, Quantum Dot Cellular Automata has come up with mentionable advancements.

The main characteristics of QCA circuits being low power consumption [4], very high integrity [5] and more importantly, size is reducible up to Nano-scale. Author's [6] shows crossbar network in QCA, makes this technology a particularly promising one. Quantum-dot cellular automata [7, 8] hold the use of binary digits and represent the digits as the electronic charge configuration within a cell.

The QCA circuits are implemented on the basis of coulombic interactions within the electrons. The ability to design the normal combinational circuits with the aid of clock pulses implies the ease of design using QCA technology. Adder and Subtractor are two basic building blocks of any arithmetic and logic circuit design. Adder designed using XOR gate is shown [9]. Multilayer concept of QCA is used [10] for modified half adder and duplicated half adder design where it took large area and more delay margin. Several studies have shown that general purpose adder, subtractor, memory and computational circuit design is possible in QCA [5, 9, 11-12]. A QCA based BCD adder circuit using 2-D wave clocking is presented [13]. One bit adder presented [14] uses two majority gates and one inverter circuit. Serial adder and ripple carry adder is shown [15] using coplanar wire crossing. Half adder and subtractor are designed [16] using F shaped XOR gate with simple clock signals. Author's [17] showed two full adders first one is in one layer and the second one is in three layers. A comparative study is made for the design. Half adder, full adder and serial adder and subtractor [18-21] are shown using majority gate and XOR gate where area consumption is more comparing to the proposed one. One bit full adder [22] is designed after proper clock assignment which the authors defined as sneak noise path elimination for the majority gate and crossover of QCA based design. A comparative study for full adders in terms of delay, temperature cell area is shown [23].

The main contribution of this is to design a robust layered controllable Adder Subtractor circuit where both the operations happen in the same circuit with the single stroke of a clock signal only. The paper proposes a

method of static power estimation of a QCA cell and also estimates the power of the proposed designs. The idea of the controllable adder subtractor circuit is applied on an arithmetic logic unit circuit and showed its robustness by the calculation of kink energy.

The rest of the paper is organized as follows, section II gives a background overview of different circuit elements and structures used in quantum dot cellular automata. Section III describes the detail of proposed work of controllable layered half and full adder circuit design using QCA technology. Section IV analyses and describes the proposed designs with calculation of latency, Area Utilization Factor (AUF) and kink energy. The results are compared with some previous designs to show the improvements. Section V describes an ALU circuit using the proposed design and the corresponding kink energy estimation and section VI concludes the paper.

II. Overview Of Quantum Dot Cellular Automata

Quantum Dot Cellular Automata as mentioned earlier is an emerging nanotechnology. The main points that are required to be discussed on this regard are QCA Cell, QCA logic gates, the Clocking of QCA circuits and the layering of QCA structure.

2.1 QCA Cell

It is the fundamental part of the QCA design. Now, in a QCA cell, four quantum dots are present at the corners of the squared structure. They are happened to be coupled with the help of tunneling barriers. In accordance to the Coulomb's law, the electrons will try to position themselves into diagonally opposite dots. The quantum dots are made with semi-conductor or metal which are having diameter small enough to get their charging energy more than k_bT (k_b=Boltzmann's constant, T=Operating Temperature). Electrons tunnel between these quantum dots but aren't allowed to leave the cell. By the means of the mechanism named Electron tunneling, the mobile electrons can occupy different quantum dots in a QCA cell. The main principle of QCA through which the data propagates in it is the effects of neighboring cell i.e. the adjacent cell electrons interact between them to affect the polarization of the electrons.

The prime methodology of QCA technology is the interaction between two bi-stable QCA cells. There are two main positions of interest in a QCA cell. These cases take place when the electrons are localized within the dots due to the high potential barriers. Due to the electrostatic repulsion between the isolated cell electrons, they can be arranged in two ways as shown in the figure which are denoted by cell polarization P = +1 or p= -1. This arrangement of cell, which does not denote the dipole moment in this case, represents encoding of binary data. According to the conventional notation, a binary 1 is denoted by P= +1 and binary 0 is represented by P= -1. The two states are happened to be energetically same until and unless the oppositely polarized cells are nearby that influence the particular cell [9]. Fig.1 shows the basic QCA cells with their polarizations.

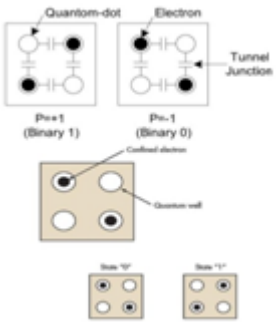

Figure1. QCA Cells and Polarizations

2.2 QCA logic gates

The basic QCA circuit is a three input majority gate voter. It is an arrangement of five cells as shown in Fig 2. The Boolean representation of the circuit is Y=AB+BC+CA, where A, B and C are the three inputs and Y happens to be the output.

Due to Coulombic interaction between the cells, the middle cell is organized according to the neighboring input cells and in terms provides the aforementioned output. Majority gate output=AB+BC+CA. Now the reason behind this majority gate being the basic building block is when one input is +1 polarized, the output is Y=A+B i.e. it represents OR gate. And when it is -1 polarized the output is Y=AB i.e. works as AND gate.

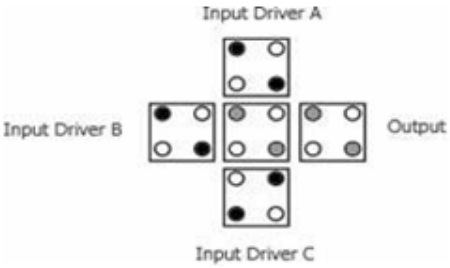

Figure2. Majority Gate circuit of QCA

2.3 Clocking in QCA

The importance of clocking is inevitable in case of QCA cells. The power consumptions and the propagation of data through the cells are mainly controlled by the clock signals. Proper usage of clock signal leads to less power consumption.

In QCA circuits, there is not any flow of current. The information passes through the cells in form of the influence of change in position of the electrons on the neighboring cells. This is the reason the clock pulses play a very important role in synchronized data flow in a QCA circuit.

The Clocking in QCA cell as shown in Fig 3 is comprised of 4 phases – switch, hold, release and relax. In the first Switch phase, the tunneling barrier begins to rise. Hold phase indicates the tunneling barrier has reached a point high enough for preventing electron tunneling. Release phase operates in reverse to the hold phase. And the final Relax phase allows electron to tunnel again by lowering the barrier potential. These four phases of clock complete one clock cycle [7, 13] which gives energy or power to the circuit to perform its operation.

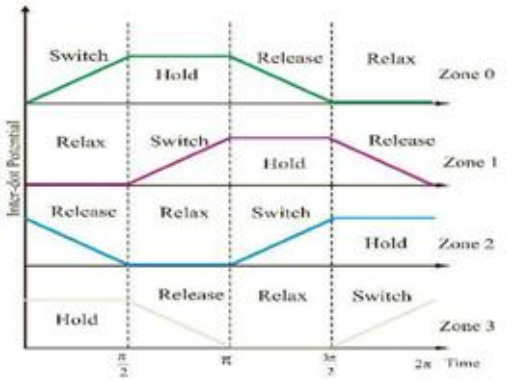

Figure3. Graphical representation of Clocking of QCA

2.4 QCA Layering

The design of QCA circuits can take place in multiple layers i.e. QCA allows to from the circuit in more than a layer. It is a huge advantage because of the fact that this can reduce the size of the devices appropriately.

Fig 4 shows the layered structure of QCA cells. Cells are placed continuously in vertical or horizontal manner [9]. The strip of a QCA cell is also known as QCA wire. So, the concept of layered design, enable us to do the Wire-crossing [8].This is very important in systematic design of logic circuits. Now, wire-crossing can take place in same plane or it can be multilayered too. In the proposed design, the concept of multilayer and wire-crossing is used for the improvement of the design compare to the previous ones.

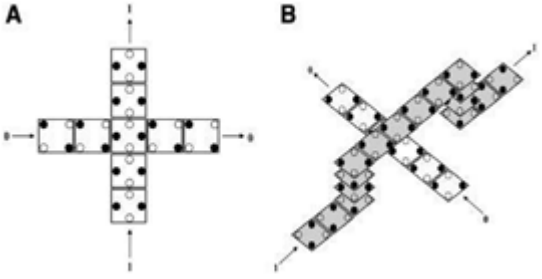

Figure4. QCA Single Layered and Multilayered Circuit Structure

III. Proposed Work

Adder and Subtractor are the pathway of the more complex designs. Half Adder was designed in a single layer as well as in multilayer too [17]. Here, in the first part of the proposed work layered half Adder and half Subtractor circuits are designed Then, a new structure of a combined circuit of half Adder and Subtractor is designed which yield all the three outputs of sum, carry and borrow at once.

One important note to be made here is that as it is known that the expression of the Sum and Difference in Adder and Subtractor circuits are the same, so here two different outputs in any case, instead kept it in a single cell.

Next the proposed work is on a controllable design of Adder and Subtractor circuit. The proposed work is a new structure of layered half and full adder circuit which will reconfigure itself in stroke of a clock pulse. QCADesigner provides the platform to analyze the design in virtual world. In this software, the designs are made and simulate accordingly to verify the potent outputs of the generated circuits. Designed circuit is compared with some previous designs. Proposed design works with correct output in a two bit multiplier ALU circuit. A novel way of static power estimation in QCA based design is shown first time in the paper. Area Utilization Factor (AUF) which is defined as the ratio of effective area of the building block under consideration to the cell area and operational cost (O-Cost) which is defined as the number of cells operating in the active device of the circuit is shown in the paper.

IV. Design and analysis of the proposed circuit

Following are the proposed designs of the adder and subtractor circuits and the corresponding outputs with the comparative study.

4.1 Layered Half Adder

Fig 5 shows layered half adder circuit consists of two layers. The lower polarization cell is placed on different layer with respect to other circuit. Simulated output the corresponding half adder circuit is shown in Fig 6.

Table 1.a shows the comparison of different circuit parameters like number of cells required, area of the design and latency for the designed circuit with some previous designed half adder circuits. Table 1b shows the calculation of area utilization factor and latency of the proposed adder circuit. Area Utilization Factor (AUF) is framed as the ratio between the total area and the net area of all occupied cells which are in use. Here L mean the total length of the circuit, width mean the total width occupied by the designed circuit, so total area is total length multiplied by total width and net area is the number of cells which are required for building the circuit multiplied by the rectangular cell dimension mean area of one cell which is taken as 18nm×18 nm.

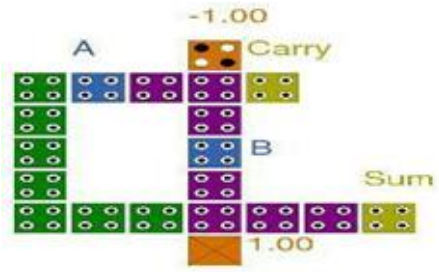

Figure5. Layered Half Adder Circuit

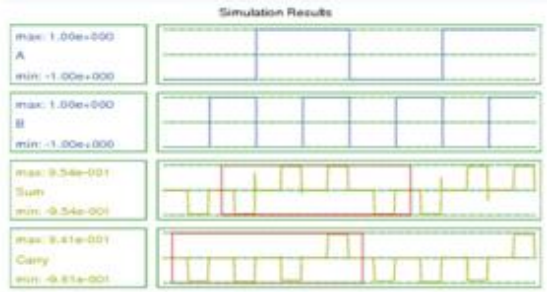

Figure6. Output of the Layered half Adder Circuit

4.2 Layered Half Subtractor

Fig 7 depicted the layered half Subtractor circuit. This circuit is similar with the previous design except both the polarizing cells are in the second layer. Simulated output of the corresponding circuit is shown in Fig 8.

In order to achieve stability of the circuit kink energy calculation is done for different inputs which are shown in Table 1c.

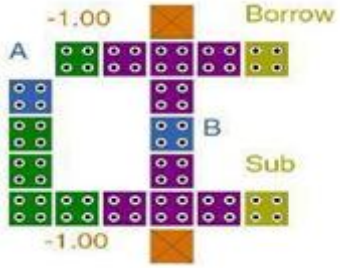

Figure7. Layered Half Subtractor Circuit

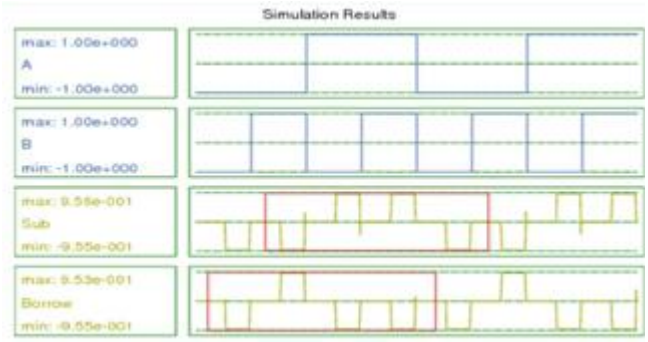

Figure 8. Layered Half Subtractor Output

Table 1a: Parameter comparison with the proposed Layered Half Adder and Subtractor circuit with the results of previous literatures

Designed circuits	Area	No of cells	Latency
Half adder designed by F Ahmed et al [9]	0.03 μm^2 and 0.06 μm^2	27 and 46	0.5 and 1
Half adder designed by Cho et al [10]	0.17 μm^2	108	3
Half adder designed by Ahmed & Khan et al [16]	0.03 μm^2	22	1
Half adder designed by S K Lakshmi et al [18]	0.08 $\mu m^2$and 0.10 μm^2	77 and 105	1
Half adder designed by J. I. Reshi et al [19]	0.0356μm^2	46	3
Proposed layered half adder	0.02 μm^2	20	0.5
Half Subtractor by Ahmed & Khan et al [16]	0.03 μm^2	19	1
Half Subtractor by S K Lakshmi et al [20]	0.0725μm^2	77	3
Half Subtractor by H. Dallaki [21]	0.0408 μm^2	55	3
Half Subtractor by J Iqbal et al [19]	0.0356 μm^2	45	3
Proposed layered half Subtractor	0.03 μm^2	19	0.5

Table 1b: Operational Cost, AUF, Latency estimation of proposed Layered Half Adder circuit

Length Covered(L)	Width Covered(W)	No of cell	Net Area	Operation cost	Total Area(L×B)	Area Utilization Factor(Total Area/ Net Area)	Latency
120nm	14nm	19	$19\times18\times18=6156nm^2$	19	16800	2.729	0.5

Table 1c: Kink Energy of the Half Subtractor Circuit

Cell name	Input	Calculations($*10^{-20}$j)
Borrow	0 0	16.516
	0 1	26.225
	1 0	26.225
	1 1	30.354
Sub	0 0	20.645
	0 1	30.354
	1 0	32.356
	1 1	35.456

Here, it is seen from the observations that the kink energy for a definite output cell does not change much due to the change in input conditions. It mostly depends upon the number of cells in a particular active clock zone and the orientations or the polarizations in the cells in those clock zones. Kink energy in the output cell is shown in Fig 9.

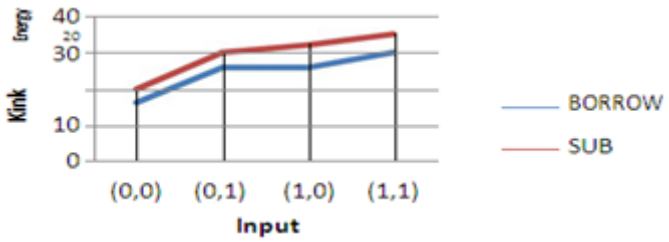

Figure9. Kink Energy in the output cells

4.3 Controllable Half Adder –Subtractor Circuit

This circuit consists of two layers. The crossover parts indicate the second layer. Here, changing the clock cycle is made at the top-left corner of the cell yields output of Half Adder and Half Subtractor in two cases. A flow chart in Fig 10 shows the functionality of the half adder-subtractor circuit for its controllable operation. Fig 11 shows the controllable half adder circuit and its corresponding output is shown in Fig 12. Fig 13 shows the controllable half Subtractor circuit and corresponding simulated output is shown in Fig14. Table 2a shows the calculation of Area Utilization Factor, number of cells required for the design, Operational Cost and Latency. Table 2b shows the corresponding kink energy calculations. Fig 15 shows the corresponding kink energy curve for the proposed controllable half adder and subtractor circuit

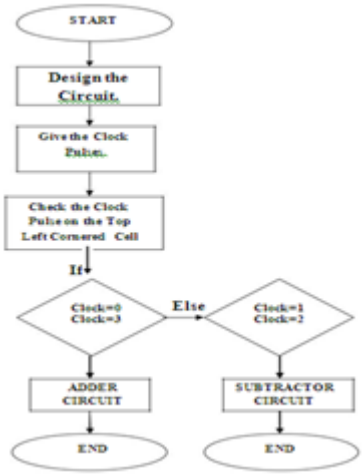

Figure10. Flow-chart of the method of Controllability in the proposed Half Adder-Subtractor Circuit

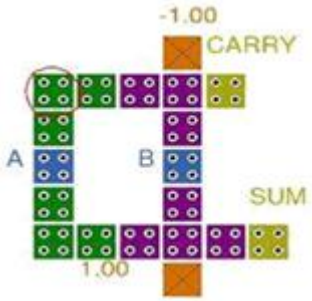

Figure11. Controllable Half Adder circuit

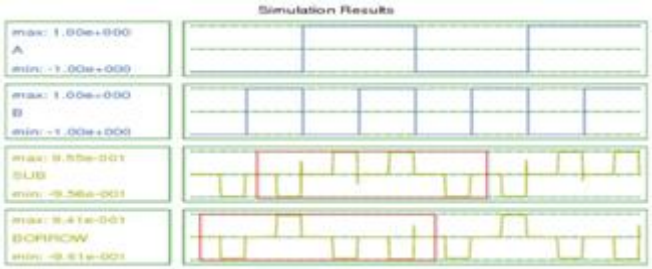

Figure12. Simulated output of Controllable Half Adder circuit.

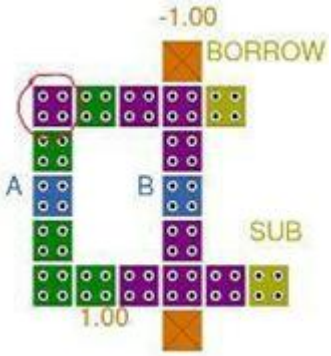

Figure13. Controllable circuit as Half Subtractor

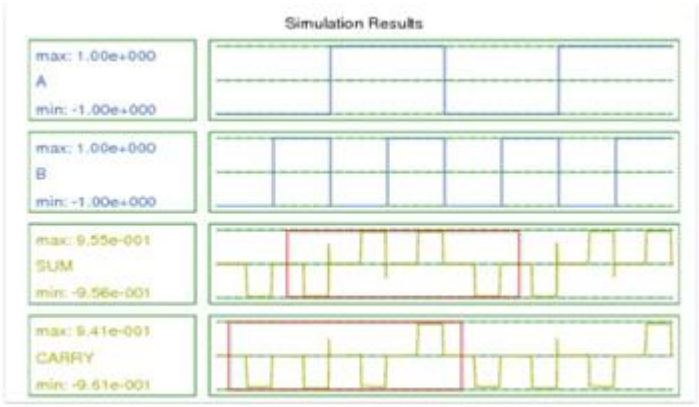

Figure14. Simulated output of Controllable Half Subtractor circuit

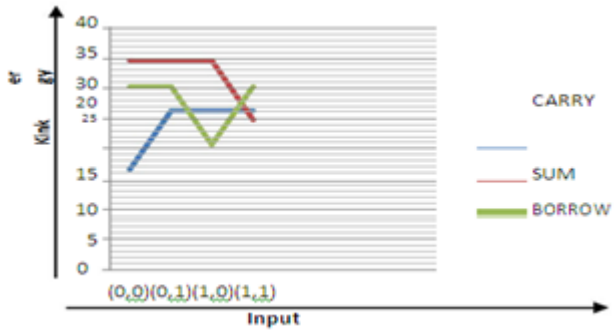

Figure15. Kink Energy in the output cells of half adder Subtractor

Table 2a: Operational Cost, AUF and Latency calculations for Controllable Half Adder-Subtractor Circuit

Length Covered(L)	Width Covered(W)	No of cell	Net Area	Operation cost	Total Area(L×B)	Area Utilization Factor(Total Area/ Net Area)	Latency
205nm	200nm	39	$39\times18\times18=12636nm^2$	39	41000	3.245	0.75

Table 2b: Kink Energy for Controllable Half Adder-Subtractor Circuit

Cell name	Input conditions	Calculations($*10^{-20}$J)
Carry	0 0	16.516
	0 1	26.225
	1 0	26.225
	1 1	26.225
Sum	0 0	34.483
	0 1	34.483
	1 0	34.483
	1 1	24.774
Borrow	0 0	30.254
	0 1	30.254
	1 0	20.645
	1 1	30.254

4.4 Controllable Full Adder –Subtractor Circuit

The concept of proposed controllability has been carried out in an extended circuit which is a little differently structured. Here, the circuit is designed in such a way that will yield the Sum-Carry and Borrow-Carry output of the Full Adder and Full Subtractor circuit respectively with the change of Clock pulse of a particular cell as shown in the following figures. Fig 16 shows the circuit named as controllable full circuit phase 1 where its output marked as for sum and carry which is shown in Fig 17. Here control cell marked with clock zero or the first applied clock in QCADesigner tool. Fig 18 shows controllable full circuit phase 2 where controlled cell marked with the clock one or the second clock of the tool. Output with carry and borrow

respectively is shown in Fig19. Table 3a shows the calculations of Area Utilization Factor, Latency and Operational Cost of the proposed circuit. Table 3b shows a comparison table of Adder Subtractor with the earlier proposed one.

Table 3c shows the kink energy estimation for different inputs for controllable full Adder-Subtractor circuit. Kink energy estimation curve for the proposed controllable full adder and Subtractor circuit is shown in Fig 20.

From the observations it shows that the kink energy [24] for a definite output cell does not change much due to the change in input conditions. It mostly depends upon the number of cells in a particular active clock zone and the orientations or the polarizations in the cells in those clock zones. Also, it is observed that the energy of the cells is independent of each other. Proposed controllable circuit is compared with the previous established circuits [18, 23, 20, 25-28] in table 3b.

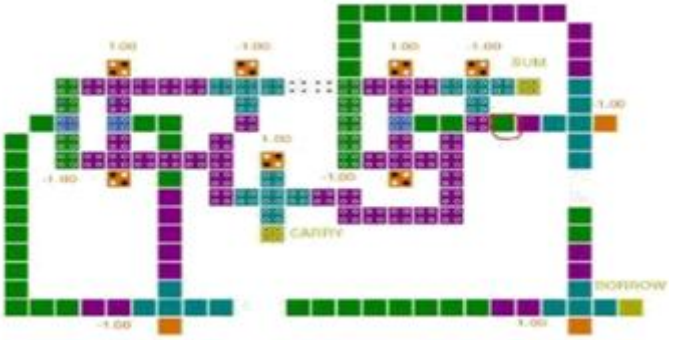

Figure16. Controllable Full Circuit Phase 1

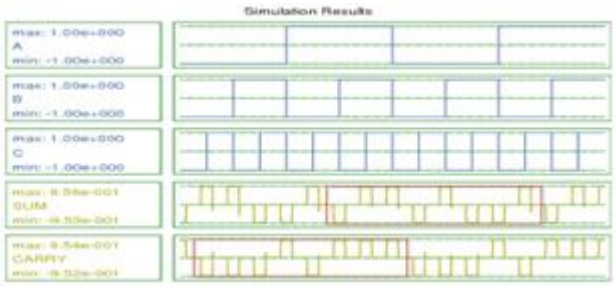

Figure17. Controllable Full Circuit Phase 1 Output (Sum and Carry)

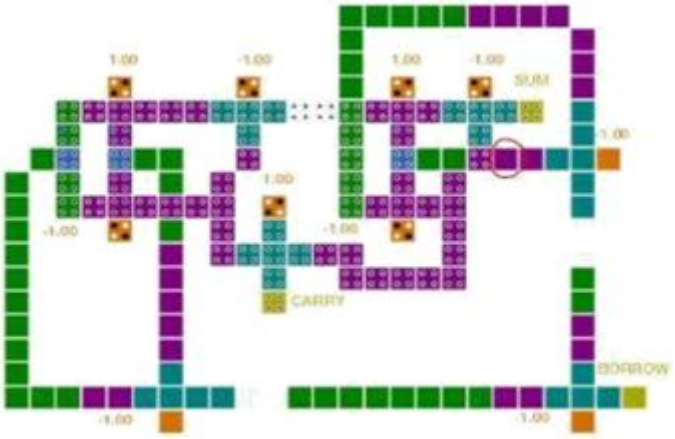

Figure18. Controllable Full Circuit Phase 2

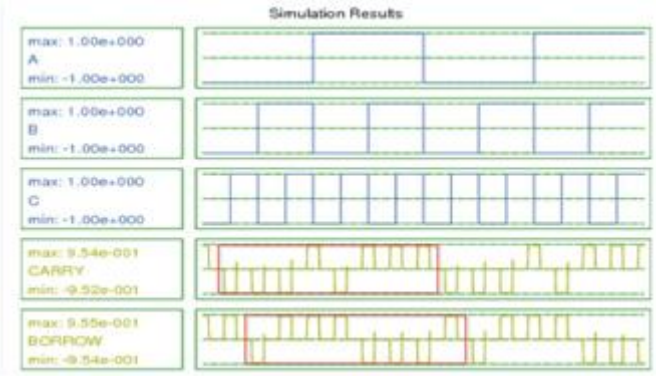

Figure19. Controllable Full Circuit Phase 2 Output (Carry and Borrow)

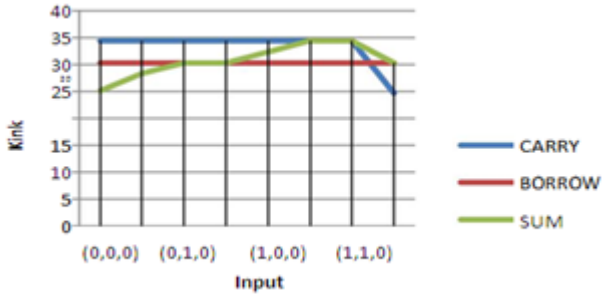

Figure20. Kink Energy in the output cells of full Adder Subtractor

Table 3a: Operational Cost, AUF and Latency calculations for proposed Controllable Full Adder Subtractor Circuit

Length Covered(L)	Width Covered(W)	No of cell	Net Area	Operation cost	Total Area(L×B)	Area Utilization Factor(Total Area/ Net Area)	Latency
500nm	360nm	154	154×18×18=49896nm^2	154	180000	3.607	2

Table 3b: Comparison between previous full adder and Subtractor devices with the proposed Controllable Full Adder Subtractor Circuit

Previous Work	Area (μm^2)	Number of cells	Latency
Full adder by K. Kyosun[22]	0.23	220	3
Full adder by S K Lakshmi et al[18]	0.208	192	2
Full adder by A. Safavi [23]	0.22	180	4
t-Adder gate by Sen et al[25]	0.28	168	4
Full adder by Keivan Naviet al [26]	0.1	96	2
Full adder by Keivan Naviet al [27]	0.04	41	0.5
Full adder by Keivan Naviet al [28]	0.09	95	1.25
Proposed full adder	0.18	154	2
Full Subtractor by S K Lakshmi et al[20]	0.1658	178	8
Proposed full Subtractor	0.18	154	2

Table 3c: Kink Energy for Full Adder-Subtractor Circuit:

Cell name	Input	Calculations($*10^{-20}$j)
Carry	0 0 0	34.483
	0 0 1	34.483
	0 1 0	34.483
	0 1 1	34.483
	1 0 0	34.483
	1 0 1	34.483
	1 1 0	34.483
	1 1 1	24.774
Borrow	0 0 0	30.354
	0 0 1	30.354
	0 1 0	30.354
	0 1 1	30.354
	1 0 0	30.354
	1 0 1	30.354
	1 1 0	30.354
	1 1 1	30.354
Sum	0 0 0	25.2
	0 0 1	28.4
	0 1 0	30.354
	0 1 1	30.354
	1 0 0	32.354
	1 0 1	34.483
	1 1 0	34.483
	1 1 1	30.354

V. Design of a 2 bit Multiplier ALU Circuit using the Proposed Adder Circuit

In this section designed controllable circuit is used to make a simple 2 bit Multiplier cum ALU circuit. ALU is a combinational circuit where output depends on input operations performed like add, subtract, AND, OR etc. The block diagram for two bit multiplier cum ALU circuit is shown in the Fig 21 and the corresponding QCA circuit design is shown in Fig 22 The working of the multiplier has been explained with the help of the following expressions- Inputs of the Multiplier are two 2 bit digits- A0B0 and B1A1. Now using simple multiplication rule the output becomes as under expressions as given below.

A0 B0
* B1 A1

A1A0 A1B0

A0B1 B1B0 *

S2 S1 S0

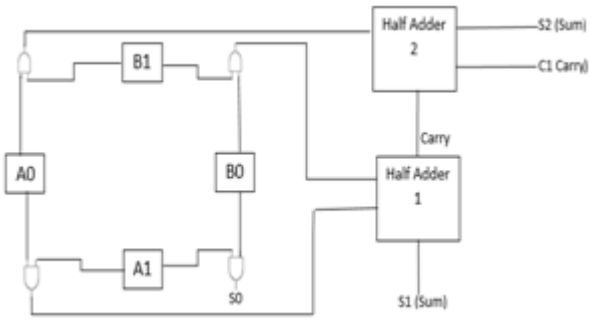

Figure21. Block Diagram of the Proposed Multiplier Circuit

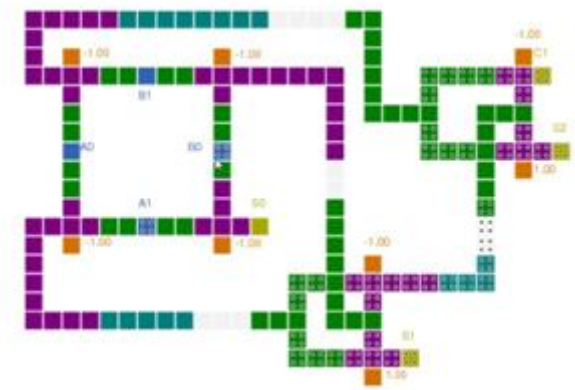

Figure22. QCA design of 2 bit Multiplier ALU circuit using the proposed Adder Circuit

The expressions of S0, S1, S2 and C1 are as follows
S0= A1B0;
S1=A1A0+B1B0;
S2=A0B1+ Carry of S1;
C1=Carry of S2;

Table 4 explained the truth table of 2 bit multiplier circuit and table 5 shows the calculations of AUF, O-cost, latency etc.

Table 4: Truth Table of 2 bit Multiplier Circuit

A0	B0	1st Input	B1	A1	2nd Input	S2	S1	S0	C1
0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	1	0	0	0	0
0	0	0	1	0	2	0	0	0	0
0	0	0	1	1	3	0	0	0	0
0	1	1	0	0	0	0	0	0	0
0	1	1	0	1	1	0	0	1	0
0	1	1	1	0	2	0	1	0	0
0	1	1	1	1	3	0	1	1	0
1	0	2	0	0	0	0	0	0	0
1	0	2	0	1	1	0	1	0	0
1	0	2	1	0	2	1	0	0	0
1	0	2	1	1	3	1	1	0	0
1	1	3	0	0	0	0	0	0	0
1	1	3	0	1	1	0	1	1	0
1	1	3	1	0	2	1	1	0	0
1	1	3	1	1	3	0	0	1	1

Simulated output of the Proposed Multiplier circuit is shown in Fig 23 which will point to the resemblance to the truth table of the ALU circuit. Fig 24 shows the corresponding kink energy plot with different inputs. Table 6 to Table 9 is the calculations for different kink energy of the ALU circuit which shows the circuit reliability and robustness of the designed circuit. Table 10 shows the parameter used in the design using QCADesigner tool [29]

Figure23. Simulated output of 2 bit Multiplier ALU circuit using the proposed Adder Circuit

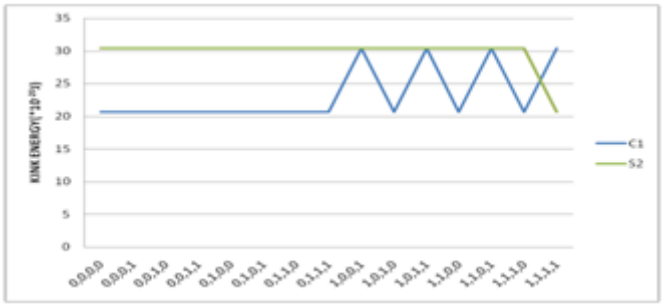

Figure24 (a) Kink Energy in the output cells c1 and s2 with different inputs

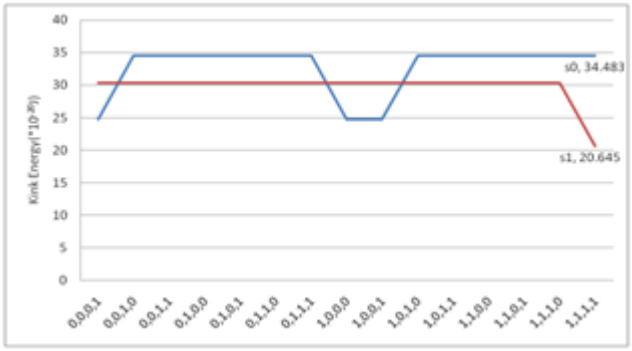

Figure24 (b) Kink Energy in the output cells s0 and s1 with different inputs.

5.1 Kink Energy Calculation of 2 Bit Multiplier ALU Circuit

To prove the robustness of the circuit kink energy calculations are done in the different output sections of the ALU circuit.

Table 5: O-Cost, AUF, Latency calculations of proposed ALU circuit

Length Covered(L)	Width Covered(W)	No of cell	Net Area	Operation cost(O-Cost)	Total Area(L×B)	Area Utilization Factor(Total Area/ Net Area)	Latency
400nm	580nm	165	$165\times18\times18=53460nm^2$	165	232000	4.34	1.5

Table6: Depicting Kink energy for carry C1

A0	A1	B0	B1	$E_{K\ AT\ C1}$ (*10^{-20}J)
0	0	0	0	20.654
0	0	0	1	20.654
0	0	1	0	20.654
0	0	1	1	20.654
0	1	0	0	20.654
0	1	0	1	20.654
0	1	1	0	20.654
0	1	1	1	20.654
1	0	0	0	20.654
1	0	0	1	30.354
1	0	1	0	20.654
1	0	1	1	30.354
1	1	0	0	20.654
1	1	0	1	30.354
1	1	1	0	20.654
1	1	1	1	30.354

Table 7: Kink energy calculations for output S0

A1	B0	$E_{K\ AT\ S0}$(*10^{-20}J)
0	0	24.774
0	1	34.483
1	0	34.483
1	1	34.483

Table 8: Kink energy for output S1

A0	A1	B0	B1	$E_{K\ AT\ S1}$ (*10^{-20}J)
0	0	0	0	30.354
0	0	0	1	30.354
0	0	1	0	30.354
0	0	1	1	30.354
0	1	0	0	30.354
0	1	0	1	30.354
0	1	1	0	30.354
0	1	1	1	30.354
1	0	0	0	30.354
1	0	0	1	30.354
1	0	1	0	30.354
1	0	1	1	30.354
1	1	0	0	30.354
1	1	0	1	30.354
1	1	1	0	30.354

Table 9: Kink energy for output S2

A0	A1	B0	B1	$E_{K\ AT\ S2}$ (*10^{-20}J)
0	0	0	0	30.354
0	0	0	1	30.354
0	0	1	0	30.354
0	0	1	1	30.354
0	1	0	0	30.354
0	1	0	1	30.354
0	1	1	0	30.354
0	1	1	1	30.354
1	0	0	0	30.354
1	0	0	1	30.354
1	0	1	0	30.354
1	0	1	1	30.354
1	1	0	0	30.354
1	1	0	1	30.354
1	1	1	0	30.354
1	1	1	1	20.645

Table 10: Parameters used in simulation of proposed QCA circuit

Temperature(Kelvin)	1.000000
Relaxation Time(sec)	1.000000e-015
Time step(sec)	1.000000e-016
Total simulation time(sec)	7.000000e-011
Clock high(J)	9.800000e-022
Clock low(J)	3.800000e-023
Clock shift	0.000000e+000
Clock Amplitude Factor	2.000000
Radius of effect	80.000000
Relative Permittivity	12.900000
Layer Separation	11.500000

VI. Conclusion

This paper proposes layered controllable half Adder Subtractor and full Adder Subtractor circuits. The designed circuit is a new concept can be used as either Adder or Subtractor according to the control input which is the clock signal in the design. Proposed design is robust and can be used where both a full adder and a full subtractor circuit is required together in nano scale, using the same device in place of two separate devices will be much cost effective. Moreover in this device, the clock signals act as the control signal, which can be changed easily to get different outputs and this can give a specific control to the manufacturer. One important design in digital electronics is ALU circuit. Here in this work a 2 bit multiplier as well as an ALU circuit is designed using the proposed adder circuit. Circuit robustness and stability is verified in different sections with different inputs by kink energy calculations. The designs are compared according to the number of cells used, area and latency with some established designed circuit.

References

[1]. *International roadmap for semiconductors* (ITRS), 2013. http://www.itrs.net.

[2]. C. S. Lent, P. D. Tougaw, W. Porod, and G. H. Bernstein, Quantum Cellular Automata, *Nanotechnology, 4*, 1993, 49–57

[3]. P. D. Tougaw and C. S. Lent, Logical devices implemented using quantum cellular automata, *Journal of . Applied. Physics, 75*, 1994, 1818-1825

[4]. R. Compano, L. Molenkamp and D. J. Paul, *Technology Roadmap for Nanoelectroincs*, 2000.

[5]. R. Zhang, K. Walus, W. Wang, and G. A. Jullien, A method of majority logic reduction for quantum cellular automata, *IEEE Transactions on Nanotechnology*, *3*, 2004, 443-450,

[6]. C. R. Graunke, D. I. Wheeler, D. Tougaw, and J. D. Will, Implementation of a crossbar network using quantum-dot cellular automata , *IEEE Transactions on Nanotechnology, 4*, 2005, 435- 440

[7]. C. S. Lent and P. D. Tougaw, A device architecture for computing with quantum dots *Proceedings of IEEE, 85*, 1997, 541–557

[8]. Craig S. Lent and Beth Isaksen, Clocked molecular quantum-dot cellular automata**,** *IEEE Transactions on Electron Devices 50 (9)*, 2003, 1890-1896.

[9]. F. Ahmad, G. M. Bhat and P. Z. Ahmad, Novel Adder Circuits Based on Quantum-Dot Cellular Automata (QCA), *Circuits and Systems*, *5*, 2014, 143-144.

[10]. Cho, H. and Swartzlender, E.E. Adder Designs and Analysis for Quantum-Dot Cellular Automata. *IEEE Transactions on Nanotechnology*, *6*, 2007, 374-383

[11]. K. Walus, T. J. Dysart, G. A. Jullien, and R. A. Budiman, QCADesigner: a rapid design and Simulation tool for quantum-dot cellular automata, *IEEE Transactions on Nanotechnology, 3*, 2004, 26-31.

[12]. Cho and E. E. Swartzlander, Jr., Adder and Multiplier Design in Quantum-Dot Cellular Automata, *IEEE Transactions on Computers*, *58*, 2009, 721-727**.**

[13]. G. Cocorullo, P. Corsonello, F. Frustaci, S. Perri,, Design of Efficient BCD Adders in Quantum-Dot Cellular Automata, *IEEE Transactions on Circuits & Systems, 64(5)*, 2017, 575-579.

[14]. M. R. Azghadi , O. Kavehei, K. Navi. A new quantum-dot cellular automata full-adder, *Microelectronics Journal*, 7, 2007, 3460-3468

[15]. I. H¨anninen and J. Takala, Robust Adders Based on Quantum-Dot Cellular Automata, *Application-specific Systems, Architectures and Processors, ASAP. IEEE*, 2007, 392.

[16]. P. Z. Ahmad, F. Ahmad and H. A. Khan, *IOSR Journal of Computer Engineering (IOSR-JCE), 16*, 2014, 11-117

[17]. M. Qanbari and R. S. Nadooshan, Two Novel Quantum-Dot Cellular Automata Full Adders, *Journal of Engineering*. 2013.

[18]. S. K. Lakshmi and G. Athisha, Design and Analysis of Adders using Nanotechnology Based Quantum dot Cellular Automata, *Journal of Computer Science*, *7*, 2011, 1072-1079.

[19]. J. I. Reshi, and M. T. Banday, Efficient Design of Nano Scale Adder and Subtractor Circuits using Quantum dot Cellular Automata, *3rd International Conference on Electrical, Electronics, Engineering Trends, Communication, Optimization and Sciences* , 2016, 89–94.
[20]. S. K. Lakshmi , G. Athisha , M. Karthikeyan and C. Ganesh, Design of subtractor using nanotechnology based QCA, *IEEE International Conference on Communication Control and Computing Technologies*, 2010, 384-388
[21]. H. Dallaki and M. Mehran, Novel Subtractor Design Based on QuantumDot Cellular Automata (QCA) Nanotechnology, *International Journal of Nanoscience and Nanotechnology*, *11,* 2014, 257-262
[22]. K. Kyosun, K. Wu, and R Karri, The robust QCA adder designs using composable QCA building blocks, *IEEE transactions on computer-aided design of integrated circuits and systems, 1*, 2007, 176-183
[23]. A. Safavi, A. Ammar, and B. M. Mosleh, An overview of full adders in QCA technology, *International Journal of Computer Science & Network Solutions, 1*, (2013) 12-35
[24]. Ratna Chakrabarty et al, Effect of Temperature and Kink Energy in Multilevel Digital circuit using Quantum dot Cellular Automata *CODEC*, 2012.
[25]. Goswami, Mrinal, Bibhash Sen, Rijoy Mukherjee, and Biplab K. Sikdar, Design of Testable Adder in Quantum-dot Cellular Automata with Fault Secure Logic, *Microelectronics Journal 60*, 2017, 1-12.
[26]. Mohammadyan, Somaye, Shaahin Angizi, and Keivan Navi. New fully single layer QCA full-adder cell based on feedback model,
[27]. *International Journal of High Performance Systems Architecture 5,(4),* 2015, 202-208.
[28]. Ahmad, Firdous, Ghulam Mohiuddin Bhat, Hossein Khademolhosseini, Saeid Azimi, Shaahin Angizi, and Keivan Navi. Towards single layer quantum-dot cellular automata adders based on explicit interaction of cells *Journal of Computational Science 16* ,2016, 8-15
[29]. Angizi, Shaahin, Esam Alkaldy, Nader Bagherzadeh, and Keivan Navi. Novel Robust Single Layer Wire Crossing Approach for Exclusive OR Sum of Products Logic Design with Quantum-Dot Cellular Automata, *Journal of Low Power Electronics 10, (2)* 2014, 259-271.
[30]. www.QCADesigner.net

IOSR Journal of Electrical and Electronics Engineering (IOSR-JEEE) is UGC approved Journal with Sl. No. 4198, Journal no. 45125.

Ratna Chakrabarty. "Design of a Controllable Adder-Subtractor circuit using Quantum Dot Cellular Automata." IOSR Journal of Electrical and Electronics Engineering (IOSR-JEEE), vol. 12, no. 4, 2017, pp. 44–59.